REMARKS

Claims 1-31 are pending. All stand rejected. Claims 1-3, 15-17, 29 and 31 are amended. The applicants request further examination and consideration in view of the amendments above and remarks set forth below.

Double Patenting Rejection:

Claims 1-31 were provisionally rejected under the judicially-created doctrine of obviousness-type double patenting in view of claims 1-26 and 28-41 of co-pending application no. 09/707,227.

Because the rejection is provisional, the applicants submit that the rejection need not be overcome unless and until it becomes non-provisional. Moreover, since the rejection was made, the claims of this application have been amended (above). Therefore, the applicants respectfully request reconsideration of the rejection in view of differences between the amended claims of this application and those of co-pending application no. 09/707,227.

Rejections under 35 U.S.C. § 102(b):

Claims 1-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Peh, "The Appia Topology Solver," (hereinafter "Peh").

As amended, the applicants' claim 1 recites as follows:

> 1. (Currently Amended) A method of designing an interconnect fabric for communication between a set of source nodes and a set of terminal nodes, comprising:
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> obtaining a design for an interconnect fabric having an interconnect device layer adjacent to either the set of source nodes or the set of terminal nodes, the interconnect device layer comprising a first interconnect device;
>
> identifying flow sets that traverse the interconnect device layer, each flow set specifying communication bandwidth between a source node of the set of source nodes and a terminal node of the set of terminal nodes and the flow sets including at least a first flow set that passes through the first interconnect device;
>
> merging a pair of the flow sets, the pair including at least the first flow set and said merging comprising adding a second interconnect device to the design, the second interconnect device being linked to the first interconnect device, thereby alleviating at least one port violation and adding an additional

interconnect device layer that includes the second interconnect device to the design; and
implementing the design.

Thus, claim 1 recites a method of designing an interconnect fabric for communication between a set of source nodes and a set of terminal nodes. A design for an interconnect fabric is obtained that includes an interconnect device layer comprising a first interconnect device. An additional interconnect device layer is then added to the design. This is accomplished by identifying flow sets that traverse the interconnect device layer. Each flow set specifies a communication bandwidth between a source node and a terminal node. At least one flow set passes through the first interconnect device. A pair of the flow sets that includes at least the first flow set is then merged. The merging comprises adding a second interconnect device to the design, the second interconnect device being linked to the first interconnect device. This results in alleviating at least one port violation.

Peh describes a "Greedy heuristic" that starts with an empty fabric and attempts to add a flow at a time in the cheapest way possible. First it tries to add a point-to-point link and, if this is not possible, it attempts to add a hub. If that again is not possible, it tries to add a switch. The heuristic fails if none of these alternatives are possible given capacity and degree constraints. Peh at pages 1-2. Peh also discloses a "Merge heuristic" that creates a terminal node for each port of a host and device. When there is more than one flow to a port, the flows are merged into an existing internal node or a new internal node. The cheapest possible switch or hub is bound to the internal node. For each internal node, other internal nodes are merged into it if possible. Peh, at page 2. Peh also discusses "future work" in which Peh states that "[t]he Greedy and Merge heuristics can be extended to handle multi-layer cascaded hubs and switch fabrics." Peh at page 3.

Thus, at page 2, Peh teaches merging flows into an internal node. However, Peh does not anticipate the applicants' amended claim 1 at least because Peh does not teach adding an additional interconnect device layer. More specifically, Peh does not teach obtaining a design for an interconnect fabric having an interconnect device layer adjacent to either a set of source nodes or a set of terminal nodes and then adding an additional interconnect device layer to the design, as is required by the applicants' amended claim 1.

While Peh discusses that "future work" may involve "multi-layer cascaded hubs and switch fabrics," Peh does not explain what is meant by this or how such a thing might be accomplished. Accordingly, Peh also does not teach the additional limitations recited in claim 1 that relate to how the additional device layer of claim 1 is added to the design. Specifically, Peh does not teach identifying flow sets that traverse the interconnect device layer or that the flow sets include at least a first flow set that passes through the first interconnect device of the interconnect device layer. Peh also does not teach merging a pair of the flow sets in which the pair includes at least the first flow set and the merging comprises adding a second interconnect device that is linked to the first interconnect device, as is required by the applicants' amended claim 1. Peh also does not teach adding an additional interconnect device layer that includes the second interconnect device to the design, as is required by the applicants' amended claim 1.

For at least these reasons, claim 1 is allowable over Peh. Claims 3-14 are allowable at least because they depend from an allowable base claim 1. Moreover, these dependent claims recite limitations not taught or suggested by Peh. For example, amended claim 2 recites merging a pair of the flow sets that does not alleviate a port violation but results in cost savings. This feature of claim 2 is supported by the applicants' specification at least at paragraph 34 and is not taught by Peh. Also, claim 3 recites repeatedly performing steps of claim 1 thereby adding more interconnect device layers to the design. Because Peh does not teach the steps of claim 1, it cannot teach repeatedly performing those steps. As another example, claim 5 recites inserting a dummy node into the interconnect device layer for each link that traverses the interconnect device layer and that is not terminated in the interconnect device layer. Nowhere does Peh teach or suggest such a feature. In addition, claim 6 recites determining for each source and terminal node one or more port violations including a number by which a set of ports for the corresponding flow sets exceed a set of available ports. In contrast, Peh teaches that when there is more than one flow to a port, the flows must be merged and coalesced into a single link. See Peh at page 2. Claims 7, 8, 9 and 10 are dependent from claim 6; this is another reason why these claims are allowable. Further, claim 7 recites that merging a pair of the flow sets alleviates at least one port violation of a source or terminal node for which the number is highest and claim 8 recites

that merging a pair of the flow sets alleviates at least one port violation of a source or terminal node for which the number is highest and also alleviates at least one port violation of a source or terminal for which the number is next highest. However, Peh does not teach or suggest ranking flow sets according to port violations. These are additional reasons why claims 7 and 8 are allowable. Claim 11 recites merging a pair of the flow sets comprises selecting pair by determining feasibility of merging the pair. However, Peh simply merges flows into an internal node without considering feasibility; at page 3, Peh states that the merge heuristic will fail if none of the fabric elements supplied can handle the capacity and degree needs of the internal node. This is another reason why claim 11 is allowable and is another reason why claims 12 and 13 are allowable, being dependent from claim 11.

As amended, the applicants' claim 15 recites as follows:

> 15. (Currently Amended) A system for designing an interconnect fabric for communication between a set of source nodes and a set of terminal nodes comprising:
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> a design for an interconnect fabric having at least one interconnect device layer that includes a first interconnect device; and
>
> a fabric design tool that modifies the design for the interconnect fabric by identifying flow sets that traverse the layer of interconnect devices, each flow set specifying communication bandwidth between a source node of the set of source nodes and a terminal node of the set of terminal nodes and the flow sets including at least a first flow set that passes through the first interconnect device, and merging a pair of the flow sets, the pair including at least the first flow set and said merging comprising adding a second interconnect device to the design, the second interconnect device linked to the first interconnect device, thereby alleviating at least one port violation and adding an additional interconnect device layer that includes the second interconnect device to the design.

Therefore, claim 15 recites a system for designing an interconnect fabric for between a set of source nodes and a set of terminal nodes. The system includes a design for the fabric and a fabric design tool that modifies the design. Similarly to claim 1, claim 15 recites that the design for an interconnect fabric includes an interconnect device layer that includes a first interconnect device. An additional interconnect device layer is then added to the design. This is accomplished by the fabric design tool identifying flow sets that traverse the interconnect device layer. Each flow set specifies a communication

bandwidth between a source node and a terminal node. At least one flow set passes through the first interconnect device. A pair of the flow sets that includes at least the first flow set is then merged. The merging comprises adding a second interconnect device to the design, the second interconnect device being linked to the first interconnect device. This results in alleviating at least one port violation.

Peh does not anticipate the applicants' amended claim 15 at least because Peh does not teach adding an additional interconnect device layer. Peh also does not teach the additional limitations recited in claim 15 that relate to how the additional interconnect device layer of claim 1 is added to the design. Specifically, Peh does not teach identifying flow sets that traverse the interconnect device layer or that the flow sets include at least a first flow set that passes through the first interconnect device of the interconnect device layer, as is required by the applicants' amended claim 15. Peh also does not teach merging a pair of the flow sets in which the pair includes at least the first flow set and the merging comprises adding a second interconnect device that is linked to the first interconnect device, as is required by the applicants' amended claim 15. Peh also does not teach adding an additional interconnect device layer that includes the second interconnect device to the design, as is required by the applicants' amended claim 15.

For at least these reasons, claim 15 is allowable over Peh. Claims 17-28 are allowable at least because they depend from an allowable base claim 15. Moreover, these dependent claims recite limitations not taught or suggested by Peh. For example, amended claim 16 recites merging a pair of the flow sets that does not alleviate a port violation but results in cost savings. This feature of claim 16 is supported by the applicants' specification at least at paragraph 34 and is not taught by Peh. Also, claim 17 recites that the fabric design tool repeatedly adds additional interconnect device layers to the design until port violations are no longer present in the design. Because Peh does not teach adding an additional interconnect device layer to the design, it cannot teach repeatedly additional interconnect device layers to the design. As another example, claim 19 recites that the fabric design tool inserts a dummy node into the interconnect device layer for each link that traverses the interconnect device layer and that is not terminated in the interconnect device layer. Nowhere does Peh teach or suggest such a feature. In

addition, claim 20 recites determining for each source and terminal node one or more port violations including a number by which a set of ports for the corresponding flow sets exceed a set of available ports. In contrast, Peh teaches that when there is more than one flow to a port, the flows must be merged and coalesced into a single link. See Peh at page 2. Claims 21, 22, 23 and 24 are dependent from claim 20; this is another reason why these claims are allowable. Further, claim 21 recites alleviating at least one port violation of a source or terminal node for which the number is highest and claim 22 recites alleviating at least one port violation of a source or terminal node for which the number is highest and at least one port violation of a source or terminal for which the number is next highest. However, Peh does not teach or suggest ranking flow sets according to port violations. These are additional reasons why claims 21 and 22 are allowable. Claim 25 recites that the design tool selects a pair of the flow sets for merger by determining feasibility of merging the pair. However, Peh simply merges flows into an internal node without considering feasibility; at page 3, Peh states that the merge heuristic will fail if none of the fabric elements supplied can handle the capacity and degree needs of the internal node. This is another reason why claim 25 is allowable and is another reason why claims 26 and 27 are allowable, being dependent from claim 25.

As amended, the applicants' claim 29 recites as follows:

> 29. (Currently Amended) A method of designing an interconnect fabric for communication between a set of source nodes and a set of terminal nodes, comprising:
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> obtaining a design for an interconnect fabric having a interconnect device layer adjacent to either the set of source nodes or the set of terminal nodes, the interconnect device layer comprising at least one interconnect device; and
>
> repeatedly forming a next interconnect device layer adjacent to either the set of source nodes or terminal nodes by identifying flow sets that traverse an existing adjacent interconnect device layer and merging a pair of the flow sets thereby alleviating at least one port violation, each added interconnect device layer comprising at least one interconnect device linked to an interconnect device of the existing adjacent interconnect device layer, thereby adding interconnect device layers to the design, until the design satisfies a set of flow requirements between the source nodes and terminal nodes without port violations.

Therefore, claim 29 recites a method of designing an interconnect fabric for communication between a set of source nodes and a set of terminal nodes. A design for

an interconnect fabric is obtained that includes an interconnect device layer comprising at least one interconnect device. A next interconnect device layer adjacent to either the set of source nodes or terminal nodes is repeatedly formed. This is accomplished by identifying flow sets that traverse an existing adjacent interconnect device layer and merging a pair of the flow sets thereby alleviating at least one port violation. Each added interconnect device layer comprises at least one interconnect device linked to an interconnect device of the existing adjacent interconnect device layer. In this way, interconnect device layers are added to the design until the design satisfies a set of flow requirements between the source nodes and terminal nodes without port violations.

As explained above, Peh does not teach adding an additional interconnect device layer. Therefore, Peh also does not teach the additional limitations recited in claim 29 that relate to how the additional device layers of claim 29 are added to the design. Specifically, Peh does not teach identifying flow sets that traverse an existing adjacent interconnect device layer and merging a pair of the flow sets as is required by the applicants' amended claim 29. Peh also does not teach that each added interconnect device layer comprises at least one interconnect device linked to an interconnect device of the existing adjacent interconnect device layer as is required by the applicants' amended claim 29. Peh also does not teach adding an additional interconnect device layers until the design satisfies a set of flow requirements between the source nodes and terminal nodes without port violations, as is required by the applicants' amended claim 29.

For at least these reasons, claim 29 is allowable over Peh. Claim 30 is allowable at least because it depends from an allowable base claim 29. Moreover, this dependent claim recites limitations not taught or suggested by Peh. Specifically, Peh does not teach that each added interconnect device layer reduces a number of port violations by at least one, thereby each added interconnect device layer progresses the design toward a condition of having no port violations, as is required by claim 30. Instead, Peh teaches that when there is more than one flow to a port, the flows must be merged and coalesced into a single link. See Peh at page 2. This is another reason why the applicants' claim 30 is allowable. Also, amended claim 31 recites merging a pair of the flow sets that does not alleviate a port violation but results in cost savings. This feature of claim 31 is supported

by the applicants' specification at least at paragraph 34 and is not taught by Peh. This is another reason why the applicants' claim 31 is allowable.

It should be noted that by distinguishing the applicants' claims from Peh, the applicants do not thereby admit that Peh qualifies as prior art.

Conclusion:

In view of the above, the applicants submit that all of the pending claims are now allowable. Allowance at an early date would be greatly appreciated. Should any outstanding issues remain, the examiner is encouraged to contact the undersigned at (408) 293-9000 so that any such issues can be expeditiously resolved.

Respectfully Submitted,

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Derek J. Westberg (Reg. No. 40,872)